FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
SP035.C5	09/329,354
APPLICANT: Garg *et al.*	
FILING DATE: June 10, 1999	GROUP: 2763

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	4,626,989	12/1986	Torii	364	200	
	AB1	4,675,806	06/1987	Uchida	364	200	
	AC1	4,722,049	01/1988	Lahti	364	200	
	AD1	4,807,115	02/1989	Torng	364	200	
	AE1	4,901,233	02/1990	Liptay	395	375	
	AF1	4,903,196	02/1990	Pomerene *et al.*	364	200	
	AG1	4,942,525	07/1990	Shintani *et al.*	395	375	
	AH1	4,992,938	02/1991	Cocke *et al.*	364	200	
	AI1	5,067,069	11/1991	Fite *et al.*	395	375	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ1	0 515 166	11/1992	EP			Yes No
	AK1	0 533 337	03/1993	EP			Yes No
	AL1	WO 91/20031	12/1991	PCT			Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	1	Acosta, Ramón D. *et al.*, "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors," *IEEE Transactions On Computers*, Vol. C-35, No. 9, September 1986, pp. 815-828.
	AN	1	Agerwala *et al.*, "High Performance Reduced Instruction Set Processors," IBM Research Division, March 31, 1987, pp. 1-61.
	AO	1	Aiken, A. and Nicolau, A., "Perfect Pipelining: A New Loop Parallelization Technique*," pp. 221-235.
	AR	1	Butler, M. and Patt, Y., "An Improved Area-Efficient Register Alias Table for Implementing HPS," University of Michigan, Ann Arbor, Michigan, January 1990, pp. 1-15.
	AS	1	Butler, M. *et al.*, "Single Instruction Stream Parallelism Is Greater Than Two," *Proceedings of ISCA-18*, May 1990, pp. 276-286.

EXAMINER: LARRY D. DONAGHUE
PRIMARY EXAMINER

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2	5,109,495	04/1992	Fite *et al.*	395	375	
	AB2	5,142,633	08/1992	Murray *et al.*	395	375	
	AC2	5,214,763	05/1993	Blaner *et al.*	395	375	
	AD2	5,222,244	06/1993	Carbine *et al.*	395	800	
	AE2	5,226,126	07/1993	McFarland *et al.*	395	375	
	AF2	5,230,068	07/1993	Van Dyke *et al.*	395	375	
	AG2	5,251,306	10/1993	Tran	395	375	
	AH2	5,261,071	11/1993	Lyon	395	425	
	AI2	5,345,569	09/1994	Tran	395	375	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ2						Yes No
	AK2						Yes No
	AL2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	2	Charlesworth, A.E., "An Approach to Scientific Array Processing: The Architectural Design of the AP-120B/FPS-164 Family," *Computer*, Vol. 14, September 1981, pp. 18-27.
	AN	2	Colwell *et al.*, "A VLIW Architecture for a Trace Scheduling Compiler," *Proceedings of the 2nd International Conference on Architectural Support for Programming Languages and Operating Systems*, October 1987, pp. 180-192.
	AO	2	Dywer, "A Multiple, Out-of-Order, Instruction Issuing System For Superscaler Processors," (All); Aug. 1991.
	AR	2	Foster *et al.*, "Percolation of Code to Enhance Parallel Dispatching and Execution," *IEEE Trans. On Computers*, December 1971, pp. 1411-1415.
	AS	2	Gee, J. *et al.*, "The Implementation of Prolog via VAX 8600 Microcode," *Proceedings of Micro 19*, New York City, October 1986, pp. 1-7.

EXAMINER: LARRY D. DONAGHUE PRIMARY EXAMINER

DATE CONSIDERED: 05/22/00

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3	5,355,457	10/1994	Shebanow *et al.*	395	375	
	AB3	5,398,330	03/1995	Johnson	395	375	
	AC3	5,442,757	08/1995	McFarland *et al.*	395	375	
	AD3	5,448,705	09/1995	Nguyen *et al.*	395	375	
	AE3	5,487,156	01/1996	Popescu *et al.*	395	375	
	AF3	5,497,499	03/1996	Garg *et al.*	395	800.73	
	AG3	5,561,776	10/1996	Popescu *et al.*	395	375	
	AH3	5,574,927	11/1996	Scantlin	395	800	
	AI3	5,592,636	01/1997	Popescu *et al.*	395	586	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ3						Yes No
	AK3						Yes No
	AL3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	3	Goodman, J.R. and Hsu, W., "Code Scheduling and Register Allocation in Large Basic Blocks," *ACM*, 1988, pp. 442-452.
	AN	3	Gross *et al.*, "Optimizing Delayed Branches," *Proceedings of the 5th Annual Workshop on Microprogramming*, October 5-7, 1982, pp. 114-120.
	AO	3	Groves, R.D. and Oehler, R., "An IBM Second Generation RISC Processor Architecture," *IEEE*, 1989, pp. 134-137.
	AR	3	Hennessy, J.L and Patterson, D.A., Computer Architecture A Quantitative Approach, 1990, Ch. 6.4, 6.7 and pg. 449.
	AS	3	Horst, R.W. *et al.*, "Multiple Instruction Issue in the NonStop Cyclone Processor," *IEEE*, 1990, pp. 216-226.

EXAMINER: LARRY D. DONAGHUE
PRIMARY EXAMINER

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4	5,625,837	04/1997	Popescu *et al.*	395	800	
	AB4	5,627,983	05/1997	Popescu *et al.*	395	393	
	AC4	5,708,841	01/1998	Popescu *et al.*	355	800	
	AD4	5,737,624	04/1998	Garg *et al.*	395	800.73	
	AE4	5,768,575	06/1998	McFarland *et al.*	395	569	
	AF4	5,778,210	07/1998	Henstrom *et al.*	395	394	
	AG4	5,797,025	08/1998	Popescu *et al.*	395	800	
	AH4	5,832,205	11/1998	Kelly *et al.*	395	185.06	
	AI4	5,832,293	11/1998	Popescu *et al.*	395	800.23	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ4						Yes No
	AK4						Yes No
	AL4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	4	Hwu, W. *et al.*, "An HPS Implementation of VAX: Initial Design and Analysis," *Proceedings of the Nineteenth Annual Hawaii International Conference on System Sciences*, 1986, pp. 282-291.
	AN	4	Hwu, W. *et al.*, "Checkpoint Repair for High-Peformance Out-of-Order Execution Machines," *IEEE Trans. On Computers*, Vol. C-36, No. 12, December 1987, pp. 1496-1514.
	AO	4	Hwu, W. and Patt, Y.N., "Design Choices for the HPSm Microprocessor Chip," *Proceedings of the Twentieth Annual Hawaii International Conference on System Sciences*, 1987, pp. 330-336, 1987.
	AR	4	Hwu, W. *et al.*, "Experiments with HPS, a Restricted Data Flow Microarchitecture for High Performance Computers," *COMPCON 86*, 1986.
	AS	4	Hwu, W. *et al.*, "Exploiting Parallel Microprocessor Microarchitectures with a Compiler Code Generator," *Proceedings of the 15th Annual Symposium on Computer Architecture*, June 1988, pp. 45-53.

EXAMINER	DATE CONSIDERED
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	AA5						
	AB5						
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	AD5						
	AE5						
	AF5						
	AG5						
	AH5						
	AI5						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ5						Yes No
	AK5						Yes No
	AL5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	5	Hwu, W. and Patt, Y.N., "HPSm, a High Performance Restricted Data Flow Architecture Having Minimal Functionality," *Proceedings of the 18th International Symposium on Computer Architecture*, pp. 297-306, June 1986.
	AN	5	Hwu, W. and Patt, Y.N., "HPSm2: A Refined Single-chip Microengine," *HICSS '88*, 1988, pp. 30-40.
	AO	5	Johnson, William M., Super-Scalar Processor Design, (Dissertation), Copyright 1989, 134 pages.
	AR	5	Jouppi *et al.*, "Available Instruction-Level Parallelism for Superscalar and Superpipelined Machines," *Proceedings of the 3rd International Conference on Architectural Support for Programming Languages and Operating Systems*, April 1989, pp. 272-282.
	AS	5	Jouppi, N.H., "Integration and Packaging Plateaus of Processor Performance," *IEEE*, 1989, pp. 229-232.

EXAMINER: LARRY D. DONAGHUE
PRIMARY EXAMINER

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA6						
	AB6						
	AC6						
	AD6						
	AE6						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ6						Yes No
	AK6						Yes No
	AL6						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	6	Jouppi, N.P., "The Nonuniform Distribution of Instruction-Level and Machine Parallelism and Its Effect on Performance," *IEEE Transactions on Computers*, Vol. 38, No. 12, December 1989, pp. 1645-1658.
	AN	6	Keller, "Look-Ahead Processors"; Dec. 1975, pp. 177-194.
	AO	6	Lam, M.S., "Instruction Scheduling For Superscalar Architectures," *Annu. Rev. Comput. Sci.*, Vol. 4, 1990, pp. 173-201.
	AR	6	Lightner *et al.*, "The Metaflow Architecture", *IEEE Micro Magazine*, June 1991, pp. 11-12 and 63-68.
	AS	6	Lightner *et al.*, "The Metaflow Lightning" Chip Set Mar. 1991 *IEEE Lightning Outlined, Microprocessor Report*, September 1990.

EXAMINER: LARRY D. DONALDSON DATE CONSIDERED: 03/27/00

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA7						
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	AH7						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ7						Yes No
	AK7						Yes No
	AL7						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	7	Melvin, S. and Patt, Y., "Exploiting Fine-Grained Parallelism Through a Combination of Hardware and Software Techniques," *Proceedings From ISCA-18*, May 1990, pp. 287-296.
	AN	7	Murakami, K. *et al.*, "SIMP (Single Instruction stream/Multiple instruction Pipelining): A Novel High-Speed Single-Processor Architecture," *ACM*, 1989, pp. 78-85.
	AO	7	Patt, Y.N. *et al.*, "Critical Issues Regarding HPS, A High Performance Microarchitecture," *The 18th Annual Workshop on Microprogramming*, Pacific Grove, California, Dec. 3-6, 1985, IEEE Computer Order No. 653, pp. 109-116.
	AR	7	Patt, Y.N. *et al.*, "HPS, A New Microarchitecture: Rationale and Introduction," *The 18th Annual Workshop on Microprogramming*, Pacific Grove, California, Dec. 3-6, 1985; IEEE Computer Society Order No. 653, pp. 103-108.
	AS	7	Patt, Y.N. *et al.*, "Run-Time Generation of HPS Microinstructions From a VAX Instruction Stream," *Proceedings of MICRO 19 Workshop*, New York, New York, October 1986, pp. 1-7.

EXAMINER LARRY D. DONAGHUE PRIMARY EXAMINER

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA8						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ8						Yes No
	AK8						Yes No
	AL8						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	8	Peleg *et al.*, "Future Trends in Microprocessors: Out-Of-Order Execution, Spec. Branching and Their CISC Performance Potential", March 1991.
	AN	8	Pleszkun *et al.*, "The Performance Potential of Multiple Functional Unit Processors," *Proceedings of the 15th Annual Symposium on Computer Architecture*, June 1988, pp. 37-44.
	AO	8	Pleszkun *et al.*, "WISQ: A Restartable Architecture Using Queues," *Proceedings of the 14th International Symposium on Computer Architecture*, June 1987, pp. 290-299.
	AR	8	Smith, M.D. *et al.*, "Boosting Beyond Static Scheduling in a Superscalar Processor," *IEEE*, 1990, pp. 344-354.
	AS	8	Smith *et al.*, "Implementation of Precise Interrupts in Pipelined Processors," *Proceedings of the 12th Annual International Symposium on Computer Architecture*, June 1985, pp. 36-44.

EXAMINER: LARRY D. DONAGHUE
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	AA9						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ9						Yes No
	AK9						Yes No
	AL9						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	9	Smith, M.D. *et al.*, "Limits on Multiple Instruction Issue," *Computer Architecture News*, No. 2, April 17, 1989, pp. 290-302.
	AN	9	Sohi, G.S. *et al.*, "Instruction Issue Logic for High Performance, Interruptable Pipelined Processors," *The 14th Annual International Symposium on Computer Architecture*, June 2-5,, 1987, pp. 27-34.
	AO	9	Swenson, J.A. and Patt, Y.N., "Hierarchical Registers for Scientific Computers," *St. Malo '88*, University of California at Berkeley, 1988, pp. 346-353.
	AR	9	Thornton, J.E., Design of a Computer: The Control Data 6600, Control Data Corporation, 1970, pp. 58-140.
	AS	9	Tjaden *et al.*, "Detection and Parallel Execution of Independent Instructions," *IEEE Trans. On Computers*, Vol. C-19, No. 10, October 1970, pp. 889-895.

EXAMINER	LARRY D. DONAGHUE PRIMARY EXAMINER	DATE CONSIDERED	03/22/00

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	AA10						
	AB10						
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	AI10						

FOREIGN PATENT DOCUMENTS

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	AJ10						Yes No
	AK10						Yes No
	AL10						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	10	Tjaden *et al.*, "Representation of Concurrency with Ordering Matrices," *IEEE Trans. On Computers*, Vol. C-22, No. 8, August 1973, pp. 752-761.
	AN	10	Tjaden, Representation and Detection of Concurrency Using Ordering Matrices, (Dissertation), 1972, pp. 1-199.
	AO	10	Tomasulo, R.M., "An Efficient Algorithm for Exploiting Multiple Arithmetic Units," *IBM Journal*, Vol. 11, January 1967, pp. 25-33.
	AR	10	Uht, A.K., "An Efficient Hardware Algorithm to Extract Concurrency From General-Purpose Code," *Proceedings of the 19th Annual Hawaii International Conference on System Sciences*, 1986, pp. 41-50.
	AS	10	Uvieghara, G.A. *et al.*, "An Experimental Single-Chip Data Flow CPU," *IEEE Journal of Solid-State Circuits*, Vol. 27, No. 1, January 1992, pp. 17-28.

EXAMINER: LARRY D. DONAGHUE PRIMARY

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA11						
	AB11						
	AC11						
	AD11						
	AE11						
	AF11						
	AG11						
	AH11						
	AI11						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ11						Yes No
	AK11						Yes No
	AL11						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	11	Uvieghara, G.A. *et al.*, "An Experimental Single-Chip Data Flow CPU," *Symposium on ULSI Circuits Design Digest of Technical Papers*, May 1990.
	AN	11	Wedig, R.G., Detection of Concurrency In Directly Executed Language Instruction Streams, (Dissertation), June 1982, pp. 1-179.
	AO	11	Weiss *et al.*, "Instruction Issue Logic in Pipelined Supercomputers," Reprinted from *IEEE Trans. on Computers*, Vol. C-33, No. 11, November 1984, pp. 1013-1022.
	AR	11	Wilson, J.E. *et al.*, "On Turning the Microarchitecture of an HPS Implementation of the VAX," *Proceedings of Micro 20*, December 1987, pp. 162-167.
	AS	11	*IBM Journal of Research and Development*, Vol. 34, No. 1, January 1990, pp. 1-70.

EXAMINER: LARRY D. DONAGHUE
PRIMARY EXAMINER

DATE CONSIDERED: 03/32/00

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